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SMITH-HILL AND BEDELL, P.C.
16100 NW CORNELL ROAD, SUITE 220
BEAVERTON, OR 97006

EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2138	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,957	FRISCH, ARNOLD M.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/05/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim.

A claim, which depends from a dependent claim, should not be separated by any claim, which does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

Claim 4 is objected to because of the following: on page 13, in line 1 of claim 4, "in accordance with claim 12" is incorrect. It should be -- in accordance with claim 3--. Appropriate correction is required.

2. Claim 12 is objected to because of the following informalities: On page 15, lines 4-5, "the first means is g the adjustable delay constant continuously supplying" is incorrect. It should be --the first means is continuously supplying--. Appropriate correction is required.

3. Claim 12 is objected to because of the following informalities: On page 15, line 10; "the constant delay or the programmable delay circuit" is incorrect. It should be -- the constant delay of the programmable delay circuit--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Dinteman (US 5,948,115).

Dinteman anticipates claim 1.

Dinteman teaches an apparatus for providing a jittery test signal for use in an integrated circuit (IC) test, the apparatus comprising: a programmable delay circuit for delaying a first signal with an adjustable delay controlled by an input digital delay word to produce a test signal, and first means for supplying a

sequence of digital data words as input to the programmable delay circuit for varying the adjustable delay so that the test signal jitters relative to the first signal (fig. 4, 6, col. 3, lines 25-33, col. 4, lines 57-63, col. 6, lines 30-51, col. 8, lines 38-62, Dinteman).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 2, 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115) as applied to claim 1 above, and further in view of Churchill et al. (US 6,006,347).

As per claim 2, Dinteman substantially teaches the claimed invention described in claim 1 (as rejected above).

However Dinteman does not explicitly teach the specific use of the apparatus wherein the programmable delay circuit resides within the IC.

Churchill et al. in an analogous art teach the integrated circuit, wherein the programmable scan circuit comprises: a logic circuit selectively decoding the scan data; and a programmable delay circuit coupled to the logic circuit (fig. 3, col. 20, lines 28-31, Churchill et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Churchill et al. by including an additional step of using the apparatus wherein the programmable delay circuit resides within the IC.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the apparatus wherein the programmable delay circuit resides within the IC would provide the opportunity to test the embedded circuits in the IC using a short signal path with less noise.

- As per claim 3, Dinteman and Churchill et al. teach the additional limitations.

Dinteman teaches the apparatus wherein the first means comprises a programmable pattern generator (fig. 6, col. 6, lines 30-34, Dinteman).

9. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115) and Churchill et al. (US 6,006,347) as applied to claim 3 above, and further in view of Adams et al. (US 5,796,745).

As per claim 4, Dinteman and Churchill et al. substantially teaches the claimed invention described in claim 3 (as rejected above).

However Dinteman and Churchill et al. do not explicitly teach the specific use of the apparatus wherein the first means resides within the IC.

Adams et al. in an analogous art teach that referring to FIG. 1, an ABIST circuit on an integrated circuit 10 in accordance with the present invention includes a programmable pattern generator circuit 100 (fig. 1, col. 3, lines 31-33, Adams et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Adams et al. by including an additional step of using the apparatus wherein the first means resides within the IC.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the apparatus wherein the first means resides within the IC would provide the opportunity to test the circuits in the IC that are not accessible through the IC's input output terminals.

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115), Churchill et al. (US 6,006,347) and Adams et al. (US 5,796,745) as applied to claim 4 above, and further in view of Osawa et al. (US 5,815,512).

As per claim 5, Dinteman, Churchill et al. and Adams et al. substantially teaches the claimed invention described in claim 4 (as rejected above).

However Dinteman, Churchill et al. and Adams et al. do not explicitly teach the specific use of the apparatus wherein the IC includes a subcircuit and wherein the apparatus further comprises: second means within the IC for selectively applying either the first signal or the test signal as an input signal to the subcircuit.

Osawa et al. in an analogous art teach that the selector circuit 233...shift mode control signal (fig. 1, col. 33, lines 57-67, Osawa et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Osawa et al. by including an additional step of using the apparatus wherein the IC includes a subcircuit and wherein the apparatus further comprises: second means within the IC for selectively applying either the first signal or the test signal as an input signal to the subcircuit.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to select the signal input to the circuit depending on the operation mode of the circuit.

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115) as applied to claim 1 above, and further in view of Osawa et al. (US 5,815,512).

As per claim 6, Dinteman substantially teaches the claimed invention described in claim 1 (as rejected above).

However Dinteman does not explicitly teach the specific use of the apparatus further comprising: means for delivering the first signal from an input terminal of the IC to the second means.

Osawa et al. in an analogous art teach that the selector circuit 233...shift mode control signal (fig. 1, col. 33, lines 57-67, Osawa et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Osawa et al. by including an additional step of using the

apparatus further comprising: means for delivering the first signal from an input terminal of the IC to the second means.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the apparatus further comprising: means for delivering the first signal from an input terminal of the IC to the second means would provide the opportunity to provide an external signal to an IC circuit.

12. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115), Churchill et al. (US 6,006,347), Adams et al. (US 5,796,745) and Osawa et al. (US 5,815,512) as applied to claim 5 above, and further in view of Takatsuka et al. (US 6,501,693 B2).

As per claim 7, Dinteman, Churchill et al., Adams et al. and Osawa et al. substantially teach the claimed invention described in claim 5 (as rejected above).

However Dinteman, Churchill et al., Adams et al. and Osawa et al. do not explicitly teach the specific use of the apparatus further comprising: second means within the IC for selectively applying either a second signal or the test signal as an input signal to the subcircuit.

Takatsuka et al. in an analogous art teach that a selector circuit...test mode (col. 12, lines 5-8, Takatsuka et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Takatsuka et al. by including an additional step of using the apparatus further comprising: second means within the IC for selectively applying either a second signal or the test signal as an input signal to the subcircuit.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the apparatus further comprising: second means within the IC for selectively applying either a second signal or the test signal as an input signal to the subcircuit would provide the opportunity to select the signal input to the circuit depending on the operation mode of the circuit.

13. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115), Churchill et al. (US 6,006,347), Adams et al. (US 5,796,745), Osawa et al. (US 5,815,512)

and Takatsuka et al. (US 6,501,693 B2) as applied to claim 7 above, and further in view of Bhawmik et al. (US 6,463,560 B1).

As per claim 8, Dinteman, Churchill et al., Adams et al., Osawa et al. and Takatsuka et al. substantially teach the claimed invention described in claim 7 (as rejected above).

However Dinteman, Churchill et al., Adams et al., Osawa et al. and Takatsuka et al. do not explicitly teach the specific use of the apparatus further comprising: third means residing within the IC for generating the first signal.

Bhawmik et al. in an analogous art teach that the pattern generator may be a BIST structure comprising part of the internal circuitry of the IC, which generates the test patterns (col. 1, lines 21-23, Bhawmik et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Bhawmik et al. by including an additional step of using the apparatus further comprising: third means residing within the IC for generating the first signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the apparatus further comprising: third means residing within the IC for generating the first signal would provide the opportunity to provide the test patterns to test circuits in the IC.

- As per claim 9, Dinteman, Churchill et al., Adams et al., Osawa et al., Takatsuka et al. and Bhawmik et al. teach the additional limitations.

Bhawmik et al. teach the apparatus wherein the third means also monitors an output signal of the subcircuit to determine whether it behaves in a particular manner while the second means applies the test signal as the input signal to the subcircuit (col. 1, lines 16-23, Bhawmik et al.).

14. Claims 10, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115) as applied to claim 1 above, and further in view of Chetlur et al. (US 6,535,014 B2).

As per claim 10, Dinteman substantially teaches the claimed invention described in claim 1 (as rejected above). Dinteman also teaches the apparatus wherein the first means alternatively continuously supplies a digital data word to the programmable delay circuit to hold the adjustable delay constant, the first

means continuously supplies a digital data word to the programmable delay circuit to hold the adjustable delay constant and the first signal input to the programmable delay circuit (fig. 6, col. 5, lines 45-46, col. 6, lines 16-20, col. 6, lines 30-34, Dinteman). Dinteman also teaches the first signal input with a period that is a function of the delay provided by the programmable delay circuit (col. 6, lines 39-43, Dinteman). However Dinteman does not explicitly teach the specific use of the apparatus that further comprises: a multiplexer for receiving a second signal and the test signal and for selectively supplying either the second signal or the test signal, wherein the test signal oscillates and the multiplexer supplies the test signal.

Chetlur et al. in an analogous art teach an integrated circuit...circuit path (fig. 1, col. 6, lines 10-24, Chetlur et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Chetlur et al. by including an additional step of using the apparatus that further comprises: a multiplexer for receiving a second signal and the test signal and for selectively supplying either the second signal or the test signal, wherein the test signal oscillates and the multiplexer supplies the test signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to selectively provide the test signal or an input signal to the signal delay circuit.

- As per claim 11, Dinteman and Chetlur et al. teach the additional limitations.

Dinteman teaches the apparatus further comprising: third means for generating data that is a function of a period of the test signal (fig. 2, 6, col. 2, lines 3-38, col. 6, lines 39-43, Dinteman).

Dinteman also teaches that the first means continuously supplies a digital data word to the programmable delay circuit to hold the adjustable delay constant (fig. 6, col. 5, lines 45-46, col. 6, lines 16-20, col. 6, lines 30-34, Dinteman).

Chetlur et al. teach that the multiplexer supplies the test signal as the first signal input (fig. 1, col. 6, lines 22-24, Chetlur et al.).

15. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115) as applied to claim 1 above, and further in view of Chetlur et al. (US 6,535,014 B2) and Osawa et al. (US 5,815,512).

As per claim 12, Dinteman substantially teaches the claimed invention described in claim 1 (as rejected above). Dinteman also teaches the apparatus wherein the first means comprises a programmable pattern generator for supplying a sequence of digital delay data words to the programmable delay circuit for varying its delay with time and for alternatively continuously supplying a digital data word to the programmable delay circuit to hold its delay constant and the first means is continuously supplying a digital data word to the programmable delay circuit to hold its delay constant (fig. 6, col. 5, lines 45-46, col. 6, lines 16-20, col. 6, lines 30-34, col. 6, lines 44-48, Dinteman).

Dinteman also teaches that the first means is supplying the sequence of digital delay words to the programmable delay circuit and for supplying the test signal as the first signal input to the programmable delay circuit (fig. 6, col. 6, lines 30-51, Dinteman).

Dinteman teaches the test signal as the first signal input to the programmable delay circuit with a period that is a function of the constant delay of the programmable delay circuit (col. 5, lines 45-47, Dinteman).

However Dinteman does not explicitly teach the specific use of the IC that includes a subcircuit, and wherein the apparatus further comprises: second means for selectively applying the test signal as an input signal to the subcircuit.

Osawa et al. in an analogous art teach that the selector circuit 233... shift mode control signal (fig. 1, col. 33, lines 57-67, Osawa et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Osawa et al. by including an additional step of using the IC that includes a subcircuit, and wherein the apparatus further comprises: second means for selectively applying the test signal as an input signal to the subcircuit.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to select the signal input to the circuit depending on the operation mode of the circuit.

Dinteman also does not explicitly teach the specific use of a multiplexer for receiving a second signal and the test signal and for supplying the second signal as the first signal input and the test signal oscillates. However Chetlur et al. in an analogous art teach an integrated circuit...circuit path (fig. 1, col. 6, lines 10-24, Chetlur et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Chetlur et al. by including an additional step of using a multiplexer for receiving a second signal and the test signal and for supplying the second signal as the first signal input and the test signal oscillates.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to selectively provide the test signal or an input signal to the signal delay circuit.

16. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115), Chetlur et al. (US 6,535,014 B2) and Osawa et al. (US 5,815,512) as applied to claim 12 above, and further in view of Churchill et al. (US 6,006,347), Adams et al. (US 5,796,745) and Takatsuka et al. (US 6,501,693 B2).

As per claim 13, Dinteman, Chetlur et al. and Osawa et al. substantially teaches the claimed invention described in claim 12 (as rejected above). Chetlur et al. also teaches the apparatus wherein the multiplexer reside within the IC (multiplexer 13 in fig. 1, col. 3, lines 9-12, line 33, Chetlur et al.). However Dinteman, Chetlur et al. and Osawa et al. do not explicitly teach the specific use of the apparatus wherein the programmable delay circuit resides within the IC.

Churchill et al. in an analogous art teach the integrated circuit, wherein the programmable scan circuit comprises: a logic circuit selectively decoding the scan data; and a programmable delay circuit coupled to the logic circuit (fig. 3, col. 20, lines 28-31, Churchill et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Churchill et al. by including an additional step of using the apparatus wherein the programmable delay circuit resides within the IC.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the apparatus wherein the programmable delay circuit resides within the IC would provide the opportunity to test the embedded circuits in the IC using a short signal path with less noise.

Dinteman, Chetlur et al. and Osawa et al. also do not explicitly teach the specific use of the apparatus wherein the programmable pattern generator resides within the IC.

Adams et al. in an analogous art teach that referring to FIG. 1, an ABIST circuit on an integrated circuit 10 in accordance with the present invention includes a programmable pattern generator circuit 100 (fig. 1, col. 3, lines 31-33, Adams et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Adams et al. by including an additional step of using the apparatus wherein the programmable pattern generator resides within the IC.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the apparatus wherein the programmable pattern generator resides within the IC would provide the opportunity to test the circuits in the IC that are not accessible through the IC's input output terminals.

Dinteman, Chetlur et al. and Osawa et al. also do not explicitly teach the specific use of the apparatus wherein the second means reside within the IC.

Takatsuka et al. in an analogous art teach that a selector circuit...test mode (col. 12, lines 5-8, Takatsuka et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Takatsuka et al. by including an additional step of using the apparatus wherein the second means reside within the IC.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the apparatus wherein the second means reside within the IC would provide the opportunity to select the signal input to the circuit depending on the operation mode of the circuit.

17. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115), Chetlur et al. (US 6,535,014 B2), Osawa et al. (US 5,815,512), Churchill et al. (US 6,006,347), Adams et al. (US 5,796,745) and Takatsuka et al. (US 6,501,693 B2) as applied to claim 13 above, and further in view of Bhawmik et al. (US 6,463,560 B1).

As per claim 14, Dinteman, Chetlur et al. and Osawa et al., Churchill et al., Adams et al. and Takatsuka et al. substantially teaches the claimed invention described in claim 13 (as rejected above). Dinteman teaches that the data is a function of a period of the test signal (fig. 2, col. 2, lines 3-38, Dinteman). Chetlur et al. also teach that the test signal oscillates (fig. 1, col. 6, lines 10-24, Chetlur et al.).

However Dinteman, Chetlur et al. and Osawa et al., Churchill et al., Adams et al. and Takatsuka et al. do not explicitly teach the specific use of the third means residing within the IC for generating data.

Bhawmik et al. in an analogous art teach that the pattern generator may be a BIST structure comprising part of the internal circuitry of the IC, which generates the test patterns (col. 1, lines 21-23, Bhawmik et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Bhawmik et al. by including an additional step of using the third means residing within the IC for generating data.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the third means residing within the IC for generating data would provide the opportunity to provide the test patterns to test circuits in the IC.

18. Claims 15, 16, 17, 18, 19, 20, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115) as applied to claim 1 above, and further in view of Saxe et al. (US 5,144,525).

As per claim 15, Dinteman substantially teaches the claimed invention described in claim 1 (as rejected above).

However Dinteman does not explicitly teach the specific use of the apparatus wherein the programmable delay circuit comprises: a plurality of buffers connected in cascade, each having an output; and a plurality of capacitive circuit elements, each corresponding to a separate one of the buffers and each providing an

adjustable capacitance at an output of its corresponding buffer, wherein the first means controls the delay of the programmable delay circuit by adjusting the adjustable capacitance provided by each of the plurality of capacitive elements.

Saxe et al. in an analogous art teach that FIGS. 11A-11E are schematic diagrams...delay line (fig. 11A-11E, 12, col. 2, lines 18-22, Saxe et al.). Saxe et al. also teach that adjustable buffer amplifier...modulates the total delay through the adjustable buffer amplifier 62D (col. 7, lines 18-29, Saxe et al.). Saxe et al. teach that the timing of the delay line...the string of buffers is achieved (col. 7, line 63-col. 8, line 1, Saxe et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Saxe et al. by including an additional step of using the apparatus wherein the programmable delay circuit comprises: a plurality of buffers connected in cascade, each having an output; and a plurality of capacitive circuit elements, each corresponding to a separate one of the buffers and each providing an adjustable capacitance at an output of its corresponding buffer, wherein the first means controls the delay of the programmable delay circuit by adjusting the adjustable capacitance provided by each of the plurality of capacitive elements.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to control the circuit elements to provide adjustable delay to a signal.

- As per claim 16, Dinteman and Saxe et al. teach the additional limitations.

Dinteman teaches the first means (prog. pattern gen. 56 in fig. 6, col. 6, lines 30-34, Dinteman).

Saxe et al. teach adjusting the adjustable capacitance of the capacitive circuit elements so that they provide substantially similar amounts of capacitance at the outputs of their corresponding buffers (fig. 11D, col. 7, lines 18-29, lines 52-56, Saxe et al.).

- As per claim 17, Dinteman and Saxe et al. teach the additional limitations.

Dinteman teaches the first means (prog. pattern gen. 56 in fig. 6, col. 6, lines 30-34, Dinteman).

Saxe et al. teach independently adjusting the adjustable capacitance of each capacitive circuit element (fig. 11D, col. 7, lines 18-29, Saxe et al.).

- As per claim 18, Dinteman and Saxe et al. teach the additional limitations.

Dinteman teaches the first means (prog. pattern gen. 56 in fig. 6, col. 6, lines 30-34, Dinteman).
Saxe et al. teach adjusting the adjustable capacitance of at least two of the capacitive circuit elements so that they provide differing amounts of capacitance at the outputs of their corresponding buffers (col. 7, lines 18-29, lines 52-62, Saxe et al.).

- As per claim 19, Dinteman and Saxe et al. teach the additional limitations.

Dinteman teaches the first means (prog. pattern gen. 56 in fig. 6, col. 6, lines 30-34, Dinteman).
Saxe et al. teach the apparatus wherein each capacitive circuit element comprises: a plurality of capacitors, and a plurality of switches controlled for coupling selected ones of the capacitors to the output of the buffer corresponding to the capacitive circuit element (fig. 11D, col. 7, lines 18-29, lines 52-62, Saxe et al.).

- As per claim 20, Dinteman and Saxe et al. teach the additional limitations.

Saxe et al. teach the apparatus wherein each capacitor is provided by an input of a gate having capacitive input impedance (fig. 11D, col. 7, lines 25-29, Saxe et al.).

- As per claim 21, Dinteman and Saxe et al. teach the additional limitations.

Dinteman teaches the first means (prog. pattern gen. 56 in fig. 6, col. 6, lines 30-34, Dinteman).
Saxe et al. teach the apparatus wherein each capacitive circuit element comprises: a plurality of gates having inputs linked to the output of the buffer corresponding to the capacitive circuit element, wherein an input capacitance of each gate is a function of a voltage applied to the gate, wherein the first means controls a magnitude of the voltage applied to each gate (fig. 11D, col. 7, lines 18-29, Saxe et al.).

19. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115) in view of Bhawmik et al. (US 6,463,560 B1).

As per claim 22, Dinteman teaches the method comprising the steps of: a. providing a programmable delay circuit having an adjustable delay controlled by digital delay control data supplied to the programmable delay control circuit; b. applying a first signal as input to the programmable delay circuit such that the programmable delay circuit delays the first signal to produce a test signal, and c. supplying a sequence of digital control data to the programmable delay circuit that varies the adjustable delay

during step b such that the test signal jitters relative to the first signal (fig. 4, 6, col. 3, lines 25-33, col. 4, lines 57-63, col. 6, lines 30-51, col. 8, lines 38-62, Dinteman).

However Dinteman does not explicitly teach the specific use of a method for testing a subcircuit of an integrated circuit (IC), the subcircuit having an input for receiving an input signal and an output for producing an output signal.

Bhawmik et al. in an analogous art teach that testing of the IC...the test patterns (col. 1, lines 16-23, Bhawmik et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Bhawmik et al. by including an additional step of using a method for testing a subcircuit of an integrated circuit (IC), the subcircuit having an input for receiving an input signal and an output for producing an output signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to test internal circuits of an IC and detect occurrence of faults.

20. Claims 23, 24, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115) and Bhawmik et al. (US 6,463,560 B1) as applied to claim 22 above, and further in view of Speyer et al. (US 6,611,477 B1).

As per claim 23, Dinteman and Bhawmik et al. substantially teaches the claimed invention described in claim 22 (as rejected above). Dinteman also teaches supplying digital delay control data to the programmable delay circuit that holds its adjustable delay constant, f. carrying out a plurality of iterations of steps d and e with the adjustable delay held to a different constant value during each iteration (fig. 6, col. 5, lines 45-47, col. 6, lines 16-20, lines 30-51, col. 8, lines 38-62, Dinteman).

However Dinteman and Bhawmik et al. do not explicitly teach the specific use of the method further comprising the steps of: d. inverting and applying the test signal as input to the circuit and, such that the test signal oscillates with a period that is a function of the adjustable delay and e. measuring the period of the test signal.

Speyer et al. in an analogous art teach that to establish the average period...the test circuit (col. 2, lines 54-58, Speyer et al.). Speyer et al. also teach that the signal propagation delay...the signal propagation time (col. 3, lines 22-27, Speyer et al.). Speyer et al. teach that test circuit 205 function as...signal transition through test circuit 205 (col. 4, lines 43-46, Speyer et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Speyer et al. by including an additional step of using the method in further comprising the steps of: d. inverting and applying the test signal as input to the circuit and, such that the test signal oscillates with a period that is a function of the adjustable delay and e. measuring the period of the test signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to provide an oscillating test signal with an adjustable delay.

- As per claim 24, Dinteman, Bhawmik et al. and Speyer et al. teach the additional limitations.

Dinteman teaches the method further comprising the step of: g. ascertaining values digital control data included in the sequence supplied at step c needed to produce a particular jitter pattern in the test signal generated at step c (col. 3, lines 25-27, col. 6, lines 39-48, Dinteman)

Speyer et al. teach the periods of the test signal measured during the plurality of iterations of step e (col. 2, lines 54-58, Speyer et al.).

- As per claim 30, Dinteman, Bhawmik et al. and Speyer et al. teach the additional limitations.

Speyer et al. teach the method wherein step e comprises counting a number of periods of a periodic reference clock signal occurring during a predetermined number of periods of the test signal (col. 2, lines 54-58, Speyer et al.).

21. Claims 25, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115) and Bhawmik et al. (US 6,463,560 B1) as applied to claim 22 above, and further in view of Churchill et al. (US 6,006,347).

As per claim 25, Dinteman and Bhawmik et al. substantially teaches the claimed invention described in claim 22 (as rejected above).

However Dinteman and Bhawmik et al. do not explicitly teach the specific use of the method wherein step a comprises the forming the programmable delay circuit within the IC.

Churchill et al. in an analogous art teach the integrated circuit, wherein the programmable scan circuit comprises: a logic circuit selectively decoding the scan data; and a programmable delay circuit coupled to the logic circuit (fig. 3, col. 20, lines 28-31, Churchill et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Churchill et al. by including an additional step of using the method wherein step a comprises the forming the programmable delay circuit within the IC.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the method wherein step a comprises the forming the programmable delay circuit within the IC would provide the opportunity to test the embedded circuits in the IC using a short signal path with less noise.

- As per claim 29, Dinteman, Bhawmik et al. and Churchill et al. teach the additional limitations.

Bhawmik et al. teach the method further comprising the step of: d. providing means within the IC for monitoring the output signal of the subcircuit to determine whether the output signal behaves in a particular manner and for sending data from the IC indicating wherein the output signal behaved in that particular manner (col. 1, lines 16-26, Bhawmik et al.).

22. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115), Bhawmik et al. (US 6,463,560 B1) and Churchill et al. (US 6,006,347) as applied to claim 25 above, and further in view of Adams et al. (US 5,796,745).

As per claim 26, Dinteman, Bhawmik et al. and Churchill et al. substantially teaches the claimed invention described in claim 25 (as rejected above). Dinteman teaches the substep c2. programming the programmable pattern generator to generate the sequence of digital delay control data (col. 6, lines 44-48, Dinteman).

However Dinteman, Bhawmik et al. and Churchill et al. do not explicitly teach the specific use of the method wherein step c comprises the substep of: c1. forming a programmable pattern generator within the IC.

Adams et al. in an analogous art teach that referring to FIG. 1, an ABIST circuit on an integrated circuit 10 in accordance with the present invention includes a programmable pattern generator circuit 100 (fig. 1, col. 3, lines 31-33, Adams et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Adams et al. by including an additional step of using the method wherein step c comprises the substep of: c1. forming a programmable pattern generator within the IC.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the method wherein step c comprises the substep of: c1. forming a programmable pattern generator within the IC would provide the opportunity to test the circuits in the IC that are not accessible through the IC's input output terminals.

23. Claims 27, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115), Bhawmik et al. (US 6,463,560 B1) and Churchill et al. (US 6,006,347) as applied to claim 25 above, and further in view of Saxe et al. (US 5,144,525).

As per claim 27, Dinteman, Bhawmik et al. and Churchill et al. substantially teaches the claimed invention described in claim 25 (as rejected above). Dinteman also teaches digital delay control data (col. 6, lines 39-48, Dinteman).

However Dinteman, Bhawmik et al. and Churchill et al. do not explicitly teach the specific use of the method wherein the programmable delay circuit comprises: a plurality of cascaded buffers connected in series, each having an output; and means for applying a capacitance of magnitude controlled by the digital delay control data to the outputs of the buffers.

Saxe et al. in an analogous art teach that FIGS. 11A-11E are schematic diagrams...delay line (fig. 11A-11E, 12, col. 2, lines 18-22, Saxe et al.). Saxe et al. also teach that adjustable buffer amplifier...modulates the total delay through the adjustable buffer amplifier 62D (col. 7, lines 18-29, Saxe et al.). Saxe et al. teach that the timing of the delay line...the string of buffers is achieved (col. 7, line 63-col. 8, line 1, Saxe et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Saxe et al. by including an additional step of using the method wherein the programmable delay circuit comprises: a plurality of cascaded buffers connected in series, each having an output; and means for applying a capacitance of magnitude controlled by the digital delay control data to the outputs of the buffers.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to control the circuit elements to provide adjustable delay to a signal.

- As per claim 28, Dinteman, Bhawmik et al., Churchill et al. and Saxe et al. teach the additional limitations.

Dinteman teaches change in value of the digital delay control data applied to the programmable delay circuit during step c (col. 6, lines 39-48, Dinteman).

Saxe et al. teach a change in the magnitude of the capacitance applied to the output of each of the cascaded buffers (fig. 11D, 12, col. 7, lines 18-29, col. 7, line 63-col. 8, line 1, Saxe et al.).

24. Claims 31, 34, 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115) in view of Bhawmik et al. (US 6,463,560 B1), Osawa et al. (US 5,815,512), Chetlur et al. (US 6,535,014 B2), Speyer et al. (US 6,611,477 B1) and Churchill et al. (US 6,006,347).

As per claim 31, Dinteman teaches a programmable delay circuit for delaying a first clock signal to with a delay selected by a digital delay control word input to the programmable delay circuit to produce a second clock signal; a programmable pattern generator for providing a sequence of delay control words as input to the programmable delay circuit (fig. 4, 6, col. 3, lines 25-33, col. 4, lines 57-63, col. 6, lines 30-51, col. 8, lines 38-62, Dinteman).

However Dinteman does not explicitly teach the specific use of a programmable delay circuit residing within the IC.

Churchill et al. in an analogous art teach the integrated circuit, wherein the programmable scan circuit comprises: a logic circuit selectively decoding the scan data; and a programmable delay circuit coupled to the logic circuit (fig. 3, col. 20, lines 28-31, Churchill et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Churchill et al. by including an additional step of using a programmable delay circuit residing within the IC.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a programmable delay circuit residing within the IC would provide the opportunity to test the embedded circuits in the IC using a short signal path with less noise.

Dinteman also does not explicitly teach the specific use of an apparatus for testing a subcircuit of an integrated circuit (IC), the subcircuit having an input for receiving an input signal and an output for producing an output signal.

However Bhawmik et al. in an analogous art teach that testing of the IC...the test patterns (col. 1, lines 16-23, Bhawmik et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Bhawmik et al. by including an additional step of using an apparatus for testing a subcircuit of an integrated circuit (IC), the subcircuit having an input for receiving an input signal and an output for producing an output signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to test internal circuits of an IC and detect occurrence of faults.

Dinteman also does not explicitly teach the specific use of the apparatus comprising: first means for selectively applying the second clock signal as the input signal to the subcircuit.

However Osawa et al. in an analogous art teach that the selector circuit 233...shift mode control signal (fig. 1, col. 33, lines 57-67, Osawa et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Osawa et al. by including an additional step of using the apparatus comprising: first means for selectively applying the second clock signal as the input signal to the subcircuit.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to select the signal input to the circuit depending on the operation mode of the circuit.

Dinteman also does not explicitly teach the specific use of a multiplexer residing within the IC for receiving a third clock signal and the second clock signal for selectively supplying either the third clock signal or the second clock signal as the first clock signal input to the programmable delay circuit.

However Chetlur et al. in an analogous art teach an integrated circuit...circuit path (fig. 1, col. 6, lines 10-24, Chetlur et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Chetlur et al. by including an additional step of using a multiplexer residing within the IC for receiving a third clock signal and the second clock signal for selectively supplying either the third clock signal or the second clock signal as the first clock signal input to the programmable delay circuit.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to selectively provide the test signal or an input signal to the signal delay circuit.

Dinteman also does not explicitly teach specifically that the second clock signal oscillates when supplied as the first clock signal input to the programmable delay circuit with a period that is a function of the delay provided by the programmable delay circuit; and a test circuit receiving the second clock signal and for generating a test signal having edges synchronized to edges of the second clock signal.

However Speyer et al. in an analogous art teach that the oscillator...the test circuit input node (col. 2, lines 51-54, Speyer et al.). Speyer et al. also teach that the signal propagation delay...the signal propagation time (col. 3, lines 22-27, Speyer et al.). Speyer et al. teach that test circuit 205 function as...signal transition through test circuit 205 (col. 4, lines 43-46, Speyer et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Speyer et al. by including an additionally that the second clock signal oscillates when supplied as the first clock signal input to the programmable delay

circuit with a period that is a function of the delay provided by the programmable delay circuit; and a test circuit receiving the second clock signal and for generating a test signal having edges synchronized to edges of the second clock signal.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to provide an oscillating test signal with an adjustable delay.

- As per claim 34, Dinteman, Bhawmik et al., Osawa et al., Chetlur et al., Speyer et al. and Churchill et al. teach the additional limitations.

Bhawmik et al. teach the apparatus further comprising: second means residing within the IC for monitoring the output signal of the subcircuit to determine whether it behaves in a particular manner in response to the test signal (col. 1, lines 16-26, Bhawmik et al.).

- As per claim 35, Dinteman, Bhawmik et al., Osawa et al., Chetlur et al., Speyer et al. and Churchill et al. teach the additional limitations.

Speyer et al. teach the apparatus further comprising: second means for counting a number of periods of a periodic reference clock signal occurring during a predetermined number of periods of the test signal (col. 2, lines 54-58, Speyer et al.).

25. Claims 32, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dinteman (US 5,948,115), Bhawmik et al. (US 6,463,560 B1), Osawa et al. (US 5,815,512), Chetlur et al. (US 6,535,014 B2), Speyer et al. (US 6,611,477 B1) and Churchill et al. (US 6,006,347) as applied to claim 31 above, and further in view of Saxe et al. (US 5,144,525).

As per claim 32, Dinteman, Bhawmik et al., Osawa et al., Chetlur et al., Speyer et al. and Churchill et al. substantially teaches the claimed invention described in claim 31 (as rejected above). Dinteman also teaches successive digital delay control word of the sequence (col. 6, lines 39-48, Dinteman).

However Dinteman, Bhawmik et al., Osawa et al., Chetlur et al., Speyer et al. and Churchill et al. do not explicitly teach the specific use of the apparatus wherein the programmable delay circuit comprises: a plurality of buffers connected in series, each having an output; and second means for adding capacitance of magnitude controlled by the sequence to outputs of the buffers.

Saxe et al. in an analogous art teach that FIGS. 11A-11E are schematic diagrams...delay line (fig. 11A-11E, 12, col. 2, lines 18-22, Saxe et al.). Saxe et al. also teach that adjustable buffer amplifier...modulates the total delay through the adjustable buffer amplifier 62D (col. 7, lines 18-29, Saxe et al.). Saxe et al. teach that the timing of the delay line...the string of buffers is achieved (col. 7, line 63-col. 8, line 1, Saxe et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dinteman's patent with the teachings of Saxe et al. by including an additional step of using the apparatus wherein the programmable delay circuit comprises: a plurality of buffers connected in series, each having an output; and second means for adding capacitance of magnitude controlled by the sequence to outputs of the buffers

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to control the circuit elements to provide adjustable delay to a signal.

- As per claim 33, Dinteman, Bhawmik et al., Osawa et al., Chetlur et al., Speyer et al., Churchill et al. and Saxe et al. teach the additional limitations.

Dinteman teaches successive delay control word of the sequence (col. 6, lines 39-48, Dinteman).

Saxe et al. teach the apparatus wherein the second means comprises: a plurality of capacitors, and a plurality of switches controlled by the sequence for selectively coupling the capacitors to inputs of the buffers (fig. 11D, col. 7, lines 18-29, lines 52-62, Saxe et al.).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Dipakkumar Gandhi
Patent Examiner

ALBERT DECADY
PATENT EXAMINER